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The Silicon Tracker of the Beam Test Engineering Model of the GLAST Large Area Telescope *

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Abstract

The silicon tracker for the engineering model of the GLAST Large Area Telescope(LAT) has at least two unique features: it employs self triggering readout electronics, dissipating less than 200 μW per channel and to date represents the largest surface of silicon microstrip detectors assembled in a tracker (2.7 m^2). It demonstrates the feasibility of employing this technology for satellite based experiments, in which low power consumption, large effective areas and high reliability are required. This note describes the construction of this silicon tracker, which was installed in a beam test of positrons, hadrons and tagged photons at SLAC in December of 1999 and January of 2000.

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1 Introduction

The principal objectives of the GLAST mission involves the observation of energetic gamma rays, starting at about 20 MeV and extending as high as TeV energies [1]. The first all–sky survey above 50 MeV was performed by the CGRO–EGRET instrument [2]. The 3^{rd} EGRET catalog contains 271 point sources, an order of magnitude more than previously known. New source classes of gamma–ray blazars and radio–quiet gamma–ray pulsars have been discovered with hints of others (millisecond pulsars, radio galaxies, supernova remnants, X–ray binaries). EGRET has raised new mysteries. There are hints of new classes of sources among the 170 sources that remain unidentified.

The GLAST Large Area Telescope (LAT) will provide overlap (50 GeV to 1 TeV) with ground–based telescopes to explore together a greatly expanded dynamic range as compared to EGRET with well–matched capabilities. It will offer tremendous opportunity for discovery in high–energy astrophysics by probing these systems with >50 times better sensitivity than previous missions. Among the main scientific objectives of the GLAST mission are to

- understand the mechanisms of particle acceleration in active galactic nuclei, pulsars, and supernovae remnants,
- determine the high energy behavior of gamma–ray bursts and transients,
- resolve the gamma–ray sky: unidentified sources and diffuse emissions,
- probe dark matter and the early universe.

The GLAST LAT, is a pair–conversion telescope consisting of a tracker/converter for direction measurement, followed by a calorimeter for energy measurement and surrounded by veto counters for cosmic–ray background rejection. The tracker employs silicon strip detectors, a modern and reliable technology commonly applied in particle physics experiments. Requirements such as reduced power consumption, self triggering electronics and large effective area (>8000 cm^2) provide a new challenge for the science community in designing a simple, yet robust experiment, that can be built in relatively short amount of time. Although the silicon detector technology has already been successfully used in space it has not relied on self triggering readout electronics [3]. A large area tracker with simple design has also been built with high detector yields in a relatively short amount of time [4].

To test the concept the GLAST collaboration has built the Beam Test Engineering Model (BTEM) that corresponds in overall size to 1/16 of the full GLAST instrument. This design meets the challenges and implements self triggering electronics with very low power consumption in the largest surface of silicon microstrip detectors built to date.

The organization of this note is as follows. Section 2 presents an overview of the silicon tracker. Section 3 offers a brief description of the design of the silicon detectors and the results from the electrical characterization. Section 4 is dedicated to ladder construction, which includes assembly, tests and mechanical survey. Section 5 describes tray construction following an organization structure similar to that of section 4. Section 6 is devoted to the tower construction. Section 7 presents an overview of the electronics and in section 8 conclusions are presented.

2 Silicon Tracker

The final LAT silicon tracker will consist of about one million readout channels, distributed over 74 m^2 of silicon with total power dissipation of less than 250 W. The silicon tracker for the test beam engineering model (BTEM), structurally corresponding to one of the sixteen towers of the GLAST LAT, consists of 41,600 readout channels. The number of detectors purchased was not sufficient to fully instrument the tracker, therefore the total silicon area is to 2.7 m^2 of silicon detectors (4% of the total area for the final LAT tracker). The construction of this tracker addresses the main issues of design reliability, validation and integration of the final instrument. Fig. 2 depicts the layout of the silicon tracker. There are 17 mechanical modules labeled trays. Each tray consists of 2 layers of detectors whose strips are oriented along the same direction. In between both layers in the same tray, near the bottom, one finds thin lead converters. Trays with strips along x and y directions alternate throughout the tracker. The topmost and bottom planes of the tracker are not instrumented with silicon detectors. To minimize degradation of the energy resolution the three bottom layers are not equipped with lead converters. Therefore, a total of 32 layers (16 planes) of single–sided silicon microstrip detectors are read out by the electronic boards mounted on the sides of the trays.

3 Silicon Microstrip Detectors

A layout of one of the corners of the BTEM silicon detector is shown in Fig. 3. The silicon detectors are single–sided, AC coupled, polysilicon biased and passivated with silicon dioxide. The strip and readout pitches are the same (194 μm) and each detector consists of 320 $p+$ strips implanted on a 400 μm–thick n type substrate. These detectors have been instrumented with aluminum lines in between implants, for by–passing of defective strips. It was not necessary to use them in the BTEM due to the good quality of the detectors.

There were 550 detectors ordered from Hamamatsu Photonics. They correspond to 296 detectors from 4–inch wafers and 254 from 6–inch wafers, whose dimensions are 64.0 mm $\times$ 64.0 mm and 64.0 mm $\times$ 106.8 mm, respectively (the final GLAST design has 89.5 $\times$ 89.5 mm^2). In addition we also received 5 detectors of 64.0 mm $\times$ 106.8 mm with the similar design manufactured by Micron Semiconductor Ltd.

The silicon microstrip detectors were tested by the manufacturer for:

- the number of defective channels (short–circuited or interrupted strips),
- leakage current as a function of the bias voltage.

In the following sections we describe the acceptance and quality control tests performed by the GLAST Collaboration.

3.1 Visual Inspections

Since the 6–inch wafer development of silicon strip detectors is still recent, all detectors were visually inspected.

Description	4–inch		6–inch		Total	
	Number	%	Number	%	Number	%
Good quality detectors	280	94.6	251	98.8	531	96.5
Runaway or unstable leakage current	1	0.3	0	0	1	0.2
Unstable current after ladder assembly	13	4.4	3	1.2	16	2.9
Losses due to mishandling	2	0.7	0	0	2	0.4
Total	296	100.0	254	100.0	550	100.0

Table 1: Summary of detector statistics for ladder assembly.

A high magnification microscope and a CCD camera were used to inspect diced detector edges. Strips were also checked for short–circuits or interrupted connections, and implants and metalization were checked for defects. All major defects were photographed. A total of 15 detectors with surface scratches will have their leakage current closely monitored for an extend period of time during and after the test beam.

3.2 Leakage Current Tests

GLAST specifications require leakage currents to be less than 50 nA/cm^2 (measured at 125 V and 25°C), which corresponds to total leakage current of about 2000 nA and 3500 nA for the detectors from 4 and 6 inch wafers, respectively. To test this, detectors were placed in light–tight probe stations in a climatized room. Each I–V curve was taken by reverse biasing the detector junctions and measuring the leakage current in steps of 10 V up to 200 V.

Fig. 4a and Fig. 4b show the distribution of the measured leakage current at a bias voltage of 100 V for 4–inch and 6–inch detectors, respectively. Only detectors with leakage current below 400 nA are displayed, corresponding to 98% (98.7%) of the total number of 4–inch (6–inch) detectors. Out of 550 detectors only 1 detector could not hold the bias voltage and had runaway leakage currents (> 10 μA) before ladder assembly. It is remarkable that the 4–inch detectors have typical leakage current of about 3 nA/cm^2, while the 6–inch detectors on average have a value of 2 nA/cm^2. Table 1 summarizes the results from detector testing in which we take a conservative approach. If a ladder draws excessive leakage current after its final assembly, for the purpose of counting, we reject all detectors in this ladder. Therefore the combined detector yield of 96.5% should be regarded as a lower limit.

4 Ladder Construction

4.1 Overview

To minimize the number of readout channels and the dead regions in the sensitive area, modules (ladders) of silicon detectors were built. Ladder construction involved the following

steps:

- assembly of detector into ladders,
- mechanical survey of the relative positions,
- electrical tests of detectors,
- wire bond of detectors,
- electrical tests on the ladder,
- encapsulation of wire bonds.

4.2 Ladder Assembly

To simplify the design of the mechanical supports, ladders have about the same length irrespective of the detector's wafer size. Ladders from 6–inch wafers are 32.04 cm long with 3 detectors connected along their shorter sides, while ladders from 4–inch wafers are 32.00 cm long and built with 5 detectors each. Before being mounted onto tray ladders are delicate objects, since only the glue along the detector edges guarantees rigidity and stability over the total length of the ladder.

Fig. 5 illustrates the fixture used for ladder assembly. Silicon detectors are mounted onto simple fixtures with Teflon pins. After the first detector is manually positioned onto the fixture, their edges are pushed against the fixture pins, which serve as a reference for the alignment. For the next detector in the ladder a very thin epoxy layer is applied along one of the edges. With the aid of a microscope the edges of two consecutive detectors are glued together. The procedure is repeated until all detectors are glued to form a ladder. After inspection of glue joints, each ladder is cured at the temperature of 60°C for 2 hours. Ladders are stored in custom made housings that are used for transport, testing and wire bonding.

4.3 Mechanical Survey of Ladders

To verify the precision of the alignment of detectors in a ladder, their relative positions were optically surveyed.

The surveying was performed using a CCD camera with magnifying optics, mounted on a measuring table. Motors moved the table in x and y, and linear encoders read its position to < 1 μm. The precision of the measurements (5.1 μm) was limited by the camera resolution ($\simeq$ 3.9 μm/pixel). A PC using a pattern recognition algorithm was used to control the movable table, to identify the fiducial marks, measure their corresponding x and y coordinates and store the measurement data to a file.

Fig. 6 shows the the straightness of the ladders due to detector alignment. The straightness of the ladder is the engineering tolerance that describes how far from a straight line the ladder is. Using fiducial marks along one side of the ladder, a least squares fit is computed

	Number of defective strips			
	Al open	Al short	Coupling short	Total
4–inch	2	2	2	6
6–inch		11	8	19
Total	2	13	10	25

Table 2: List of defective strips for all detectors.

and the maximum deviation from this line are calculated. The average of the maximum deviation from straight lines is found to be 22 μm.

4.4 Electrical Measurements

The ladder testing involved measurements of:

- the I–V curve of each detector after being glued onto a ladder,
- the I–V curve of the ladder after wire bonding,
- the capacitance of each strip after wire bonding.

The leakage current measurement follows the same procedures described in section 3.2. Out of 139 ladders, 3 show a leakage current greater than 50 nA/cm^2 and two were not assembled into trays. The third one was used to check the effect on the electronics. The reason for the increase in current is under investigation. The only noticeable change in the leakage current (about a factor of 2) occurs after wire bonding. This result is consistent with measurements from other silicon trackers. Nevertheless after wire bonding we obtain on average a total leakage current of only 3 nA/cm^2. The leakage current for all ladders after final assembly is shown in Fig. 7.

The coupling capacitance of each strip was measured on all the ladders after wire bonding. The measurements were performed with an LCR meter at 100 kHz. An automatic probe station was used to step one strip after another over 320 strips on a ladder. The coupling capacitance measurement allows us to identify a broken coupling capacitor, an electric short between aluminum strips, a break on an aluminum strip or a missing wire bond. Measured capacitance was ≈ 1.8 nF for a normal strip, an order of μF for a strip with a broken coupling capacitor, $(n+1) \times 1.8$ nF for a strip shorted to n neighboring strips, and a fraction of 1.8 nF for a broken aluminum strip.

If a broken coupling capacitor or a short between strips is identified, the ladder is repaired by removing a bonding wire from a detector with the problem. For a broken aluminum strip, no repair is carried out. Table 4.4 displays the number of defective channels for all ladders after being fully assembled. Only 25 defective strips were found for the entire tracker and it corresponds to less than 0.06% of the total number of channels.

4.5 Ladder Repair

Out of 139 ladders, 6 had to be repaired. In one of the ladders a substantial increase in leakage current was measured on the last detector. Since wire bonds were not yet encapsulated, this detector was removed and replaced. In three other ladders some encapsulation glue migrated to the backside of the detectors and these ladders were eventually glued onto the storage shelf. Two of these could be removed from the shelf and had their backplane cleaned. The remaining ladder had one of its detectors broken during this operation but it was still used for final assembly. One ladder had two detectors completely separated at the glue joints before bonding and were re–glued without problems and a second ladder was rejected due to a large misalignment (> 100 μm). Both problems may be related to their removal from the oven before the glue was completely cured. The repairs described in the following paragraphs are responsible for changing the ladder yield from 93.2% to 97.7% (include 3 rejected as described in the previous section).

5 Tray Construction

5.1 Overview

Once ladders have been built they are mounted onto support structures named trays. Tray construction involved the following steps:

- assembly of parts to form a tray,
- attachment of tested readout electronics,
- wire bonding of the readout electronics to the kapton interconnect,
- electrical testing of the tray,
- encapsulation of wire bonds,
- assembly of tested ladders onto the tray,
- wire bond of detectors to the kapton interconnect,
- mechanical survey of ladders on the tray,

5.2 Mechanical Assembly

Fig. 8 shows a schematic drawing of a BTEM tray. The support structure consists of a vented honeycomb aluminum core with 1 cm cells and 25 μm thick walls surrounded by a machined aluminum closeout frame and 75 μm thick carbon face sheets. Face sheets are glued onto the closeout and core using epoxy. Once glued they are kept under pressure for 24 hours and cured at room temperature. Large holes in the closeout frame serve to minimize the material and to vent the tray structure. The closeout has a post at each corner to define

the alignment with trays above and below. The posts are drilled to accept hollow alignment pins and Vectran tensioning cables, which pass vertically through all of the trays to compress the structure. The closeouts support the electronic boards on the sides and include bosses to which the side walls are attached. Heat flows from the electronics into the closeouts and then into the walls. A matrix of thin lead sheets with the same active area as the silicon detectors is glued onto the bottom of each tray.

Kapton flex circuits are then glued onto the top and bottom faces of the tray to route the bias voltage for the detectors. The flex circuit also includes a hatched ground plane to isolate the detector bias from possible noise in the tray structure. A tongue along one edge of the flex circuit extends over the edge of the tray. It is glued to the electronics boards and contains the narrow (100 μm) traces that carry signals from the detectors to the readout chips. The copper traces are plated with 1 μm of Ni and 0.5 μm of Au in order to accommodate wire bonding.

5.3 Tray Assembly

Tray assembly includes two different phases: electronics and detector mounting. First, tested electronics boards are mounted on two of the narrow edges of the trays (see Fig. 9). Since bond pads from the readout chips are positioned orthogonally to the plane of the detector pads, the former are initially assembled in the same plane as the detectors. After the chips are wire bonded to the kapton, leads are encapsulated. The electronics board is bent down and attached with screws onto the aluminum closeout (see Fig. 9). A set of fixtures is used for attachment, bending and encapsulation of wire bonds.

After the electronics board has been mounted, the tray is positioned onto a fixture that uses the corner posts for positioning and alignment of detectors (see Fig. 10). The first ladder is manually positioned against locators A and B. The remaining ladders are placed onto the tray at equal distance with the aid of 200 μm thick plastic shims. Ladders are attached to the kapton circuit with silver filled conductive epoxy. The glue cures in 5 hours after which the ladders are wire bonded.

The number of detectors purchased was not sufficient to fully instrument all trays. While every layer of each tray is fully instrumented with three ladders in the same given corner, some of the layers have more than three ladders. As discussed before, the topmost and bottommost tray surfaces do not contain silicon detectors. The lowest three converter layers use lead foils of 25% radiation length, rather than 3.5% to improve the effective area for measurements of high energy photons. The layout is described in Table 3.

5.4 Electrical Measurements

After the electronics boards are mounted and before loading trays with silicon, a logic analyzer controlled with the LabVIEW software[‡] is used to send signals to check the integrity of the readout. After trays are completely assembled their leakage current are measured. No significant changes have been observed.

[‡]NATIONAL INSTRUMENTS.

5.5 Mechanical Survey of Trays

All three dimensions were surveyed. The device used to measure the alignment of ladders (see Section 4.3) was modified to allow for the measurement of the z coordinate. A potentiometer was attached to a knob that controls the focusing of the image generated by the camera. An electrical signal from the camera was read out and the z coordinate was measured to an accuracy of $\pm$ 35 μm. The fiducial marks on the detectors were measured for every plane with respect to the plane formed by the tips of the four corner posts on the opposite side of the tray. The average value was $\sigma_z = \pm$ 45 μm, which includes the 35 μm measurement accuracy error.

The ladders are found to be straight with average maximum deviations from a straight line on the order of 22 μm. The ladders must be placed onto the tray parallel to the line joining the corner posts. The measured angle of rotation with respect to this line for all mounted ladders is shown in Fig. 11. The rotation is centered at 0.008° with a sigma of 0.011°. An angle of 0.01° corresponds to a run out of about 55 μm over the length of the tray. Fig. 12 shows the difference between nominal and measured positions in y with $\sigma_y = \pm$ 8 μm.

These results could be heavily influenced by errors in the measurement of the corner post location. To study this, we translated each set of ladders in a layer so that the average of the differences between the measured and nominal fiducial positions was zero, and rotated it with respect to the measuring apparatus to minimize the rms of the y differences. Then we obtained $\sigma_y = \pm$ 24 μm, as compared to $\sigma_y = \pm$ 50 μm when these rotations were not removed.

6 Tower Construction

Seventeen tray modules were stacked on each other to form a tower with 16 x,y planes of silicon detectors. As shown in Fig. 2 position 17 corresponds to the top of the tower. The description of the number of detectors and the amount of lead converter in each tray is found in Table 3. The bottom tray had an extra flange for attaching to a base plate. After the bottom tray was mounted, alignment pins and spacers were placed in the four corner holes to register the next tray. The second tray was positioned by two people holding two corners each and slowly lowered over the four alignment pins. All remaining trays were stacked successively with spacers and alignment pins in between each tray. Alternating trays were rotated 90 degrees to become either x or y tracking planes. After all the trays were stacked a 0.6 mm Vectran cable was threaded through holes in corner posts, tensioned to about 12 kg., and crimped. The Vectran cables hold the entire stack in alignment during electrical cabling and when mounting the tower walls. Two thin (0.4 mm) Kapton cables run down each tower wall, connect to the hybrid circuit boards, bend under the base plate, and feed into small repeater boards. Finally, 1.5 mm aluminum walls are screwed onto the 4 sides of the tower.

After the tower was assembled, it was optically surveyed along the z direction by the SLAC metrology group. The trays (Al closeouts) were measured to be within $\pm$ 100 μm of

			Sides of a Tray			
Stack Position	Lead Converter		Top		Bottom	
	Thickness (cm)	X_0 (%)	# Ladders	Type	# Ladders	Type
17	0.02	3.5	0	-	3	4–inch
16	0.02	3.5	3	4–inch	3	4–inch
15	0.02	3.5	2	4–inch	3	4–inch
			1	6–inch	0	-
14	0.02	3.5	3	4–inch	3	4–inch
13	0.02	3.5	3	4–inch	3	4–inch
12	0.02	3.5	3	4–inch	3	4–inch
11	0.02	3.5	3	4–inch	3	4–inch
10	0.02	3.5	3	4–inch	3	4–inch
9	0.02	3.5	4	6–inch	5	4–inch
8	0.02	3.5	5	6–inch	5	6–inch
7	0.02	3.5	5	6–inch	5	6–inch
6	0.16	25	5	6–inch	5	6–inch
5	0.16	25	5	6–inch	5	6–inch
4	0.16	25	5	6–inch	5	6–inch
3	0.0	0	5	6–inch	5	6–inch
2	0.0	0	5	6–inch	5	6–inch
1	0.0	0	5	6–inch	0	-

Table 3: BTEM Tower configuration (differs from final GLAST LAT tower design in some details).

their nominal positions. Between the bottommost tray and the tray above it there was an imperfection that did not allow them to seat properly. After correcting for that, the rest of the planes are parallel to each other within 12 μm over the length of the tray.

7 The Front–End Electronics

The main requirements for the front–end readout electronics are:

- Noise occupancy of less than 5×10^{-5} with 99% or greater efficiency for minimum–ionizing particles,
- low power ($< 240\,\mu$W per channel),
- self triggering,
- compact, to minimize intermodule dead space,
- redundancy in the readout scheme, to avoid single–point failures,
- radiation hard to 10 kRad, plus resistance to single–event latchup (to $>$ 20 MeV-cm^2/mg LET),
- resistance of configuration registers to single–event upset to a level of at least 3 pC,
- and able to sustain a 10 kHz trigger rate with <10% dead time.

The readout electronics are located on a hybrid circuit consisting of an 8–layer FR4–based printed circuit, surface mount components, and IC chips mounted directly onto the board. The boards have a soft gold body, with 0.5 μm of gold on top of 1.3 μm of nickel. Each board is located on the edge of a tray in order to minimize the dead space between adjacent tracker tower modules. Eight such boards are found on each of the 4 sides of the tracker module. Each hybrid holds twenty–five 64–channel CMOS readout ASICs, for the 1600 strips in the five ladders of a single layer. The readout ASICs have a single discriminator for each channel, with the common threshold set by a single on–chip DAC. Two masks allow selected noisy channels to be removed from the trigger output and/or the data output. Upon receipt of a trigger, the chip latches the discriminator outputs into an 8–event deep FIFO buffer to await readout.

During a readout sequence, binary data flow from one chip to the next to the end of the hybrid, with data from individual chips suppressed if the chip contains no hits for the event being read. The data flow into a CMOS digital readout–controller ASIC, where a list of addresses of hit strips is formed. Finally, the readout–controller chips send the data, one after another, down the readout cable to the VME–based data acquisition board.

The tracker trigger is based upon signals derived from logical ORs of all 1600 channels in a single layer. First, coincidences of the two layers in each x, y pair are formed. Then 3 such consecutive pairs are required to be in coincidence to form a trigger.

There is a cable connection and readout controller chip at each end of each hybrid, for redundancy. On a hybrid, either controller chip can set up and control any or all of the readout chips. Furthermore, data and trigger output signals can flow in either direction on the hybrid, or the readout can be split between any pair of readout chips, with data flowing in both directions.

The hybrids were assembled by an industrial vendor. After the surface mount components were soldered, the boards were tested by the GLAST collaboration and then returned to the vendor for mounting and wire bonding of the IC chips. The IC chips were tested by us in an automatic probe station before dicing of the wafers. All 64 channels and all 8 buffers on each chip were required to be functional for acceptance. All functional testing and any necessary repairs were carried out by us, followed by 7 days of burn–in, during which time the hybrids were powered and subjected to continual readout sequences. Details of the amplifier design and performance may be found in [5]. The electronics performed to specifications throughout the beam test, including self triggering. The noise occupancy was well below 10^{-5} at the nominal $\approx 1.4\,\mathrm{fC}$ threshold, with the exception of one noisy ladder that had to be operated at twice this threshold. With beam–test data we verified that at the nominal threshold the detection efficiency is greater than 99% within the fiducial area of the silicon–strip detectors. No problems were found with external noise pickup or common–mode noise. Details of the electronics and their performance will be published in a separate paper.

8 Conclusion

We described a beam test engineering model for the GLAST LAT silicon tracker. It was built with good quality silicon detectors with leakage current of the order of 3 $\mathrm{nA/cm^2}$. After final assembly no significant increase in leakage current has been seen and a very low number of defective channels (0.06%) was obtained.

Detectors were aligned in ladders with a precision of about 22 μm. However, the precision of assembly of ladders into trays will have to be improved to better than 50 μm. After stacking trays, the aluminum closeouts were measured to be within $\pm$ 100 μm of their nominal positions, and planarity of about 12 μm over the length of the tray was achieved.

The electronics noise occupancy was well below 10^{-5} at the nominal threshold ($\approx 1.4\,\mathrm{fC}$) with hit detection efficiency greater than 99% within the fiducial area of the silicon–strip detectors.

The construction of the BTEM silicon tracker demonstrates the feasibility of employing this technology for satellite based experiments, in which low power consumption, high reliability and large effective areas are required.

Acknowledgments

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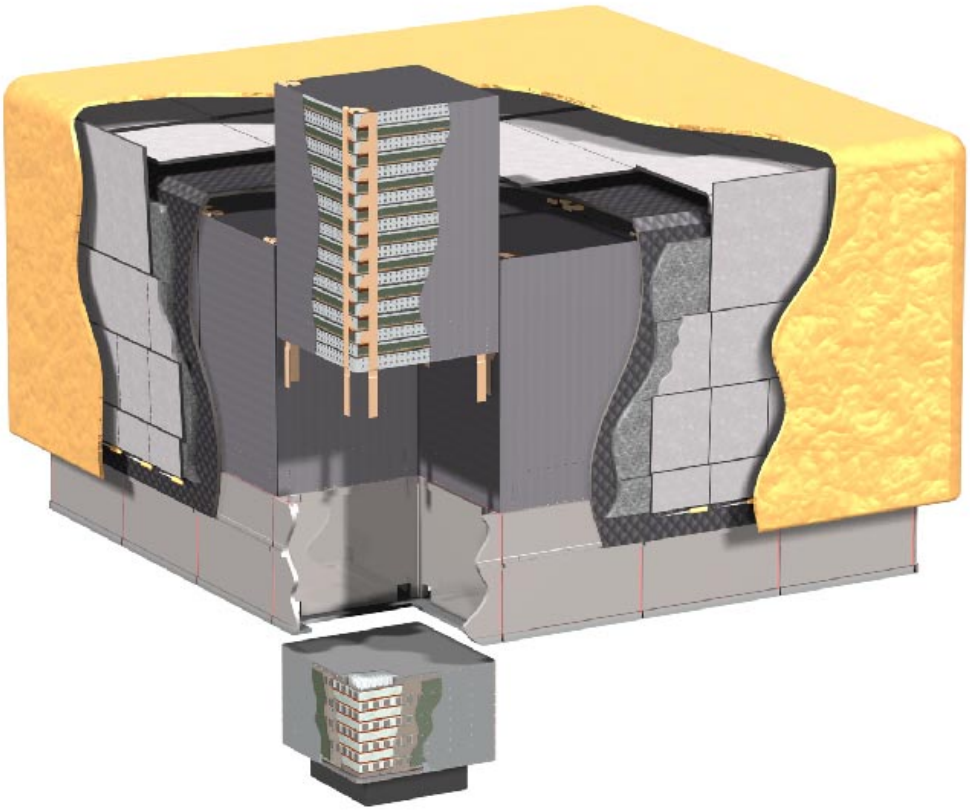

Figure 1: Exploded view of the GLAST LAT instrument.

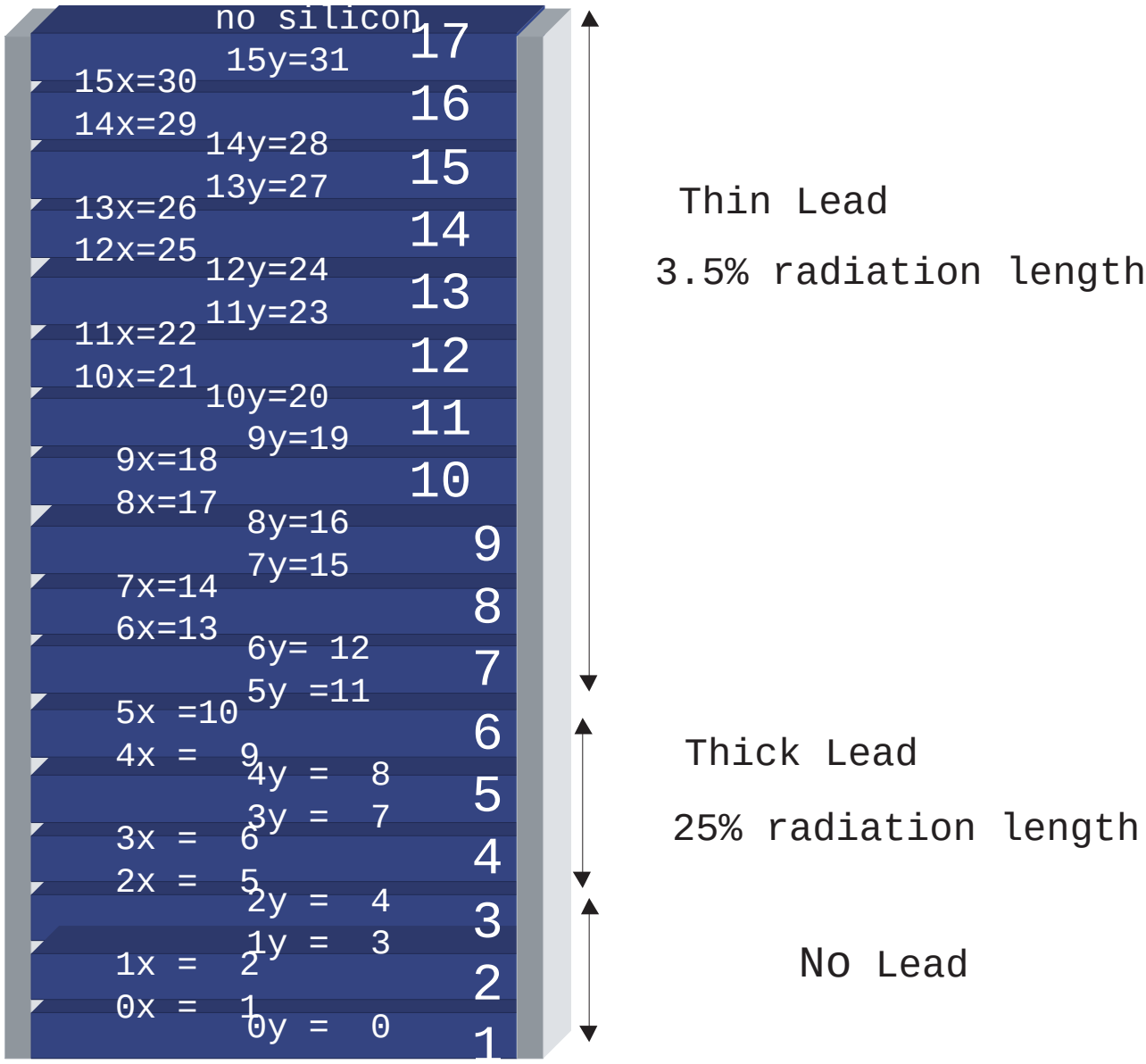

Figure 2: Schematic drawing of the GLAST LAT silicon tracker.

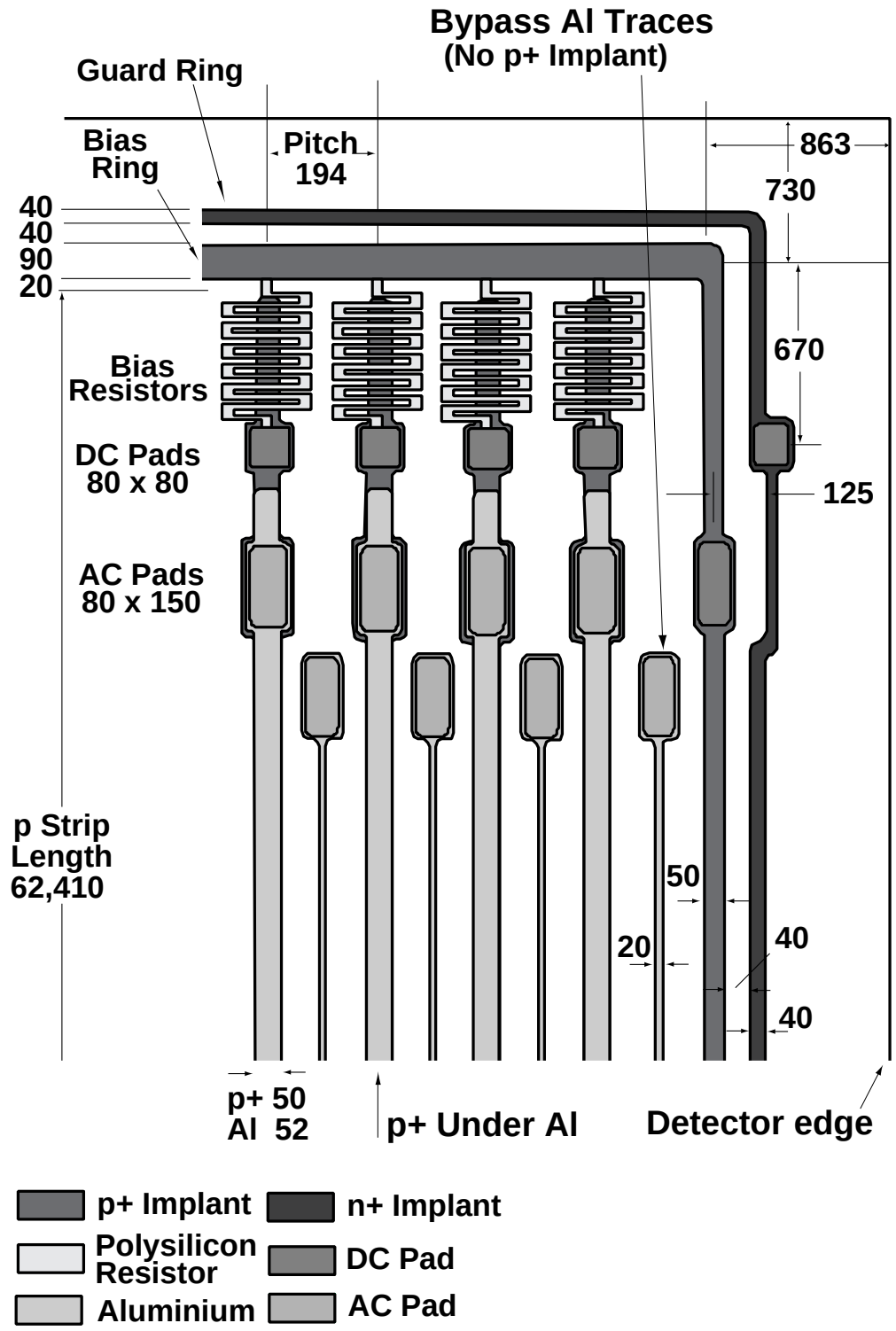

Figure 3: Layout of one corner of the silicon detector. Dimensions are in μm.

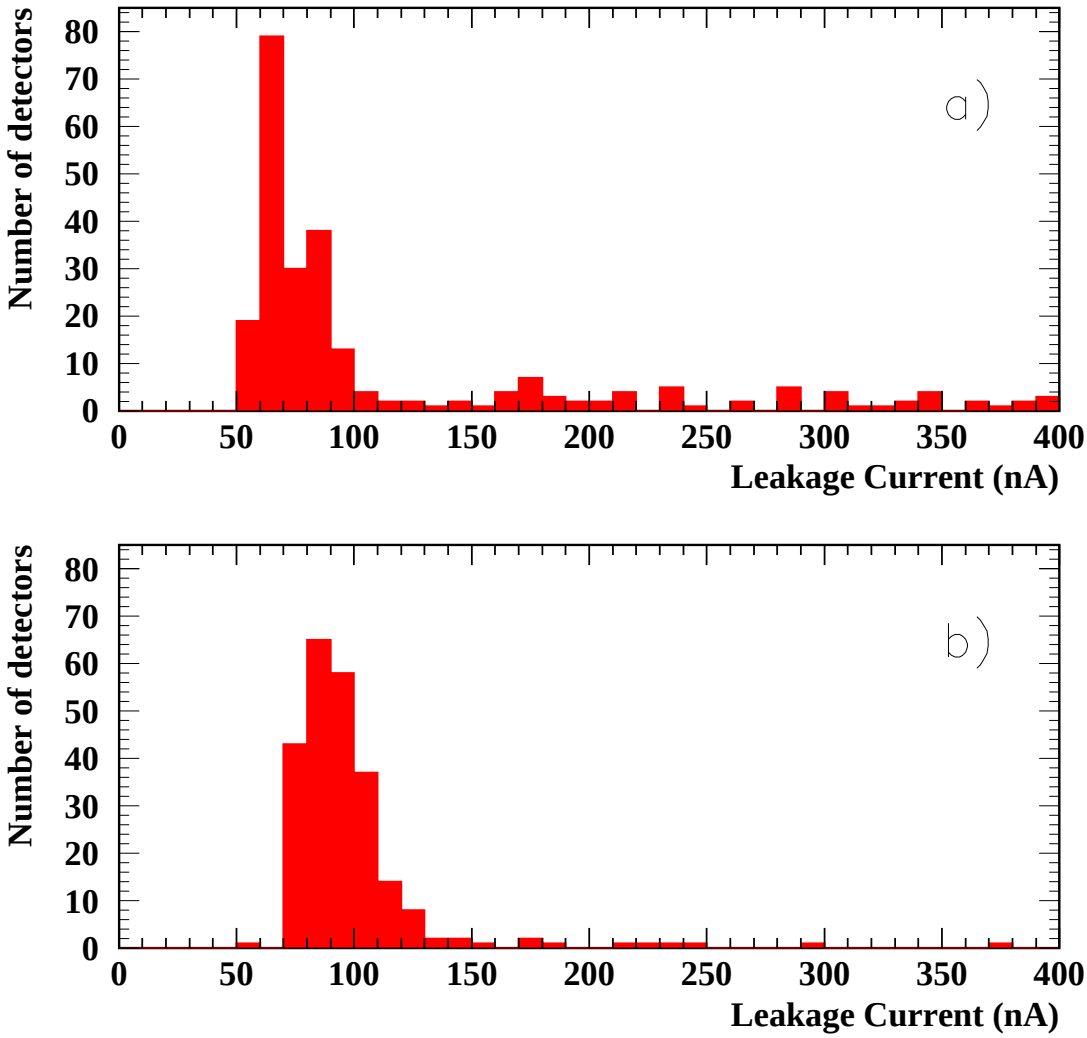

Figure 4: Measured leakage current at 100 V for all Hamamatsu detectors a) 4–inch, b) 6–inch. Only detectors with leakage current values below 400 nA are displayed, corresponding to about 98% of the total number of detectors.

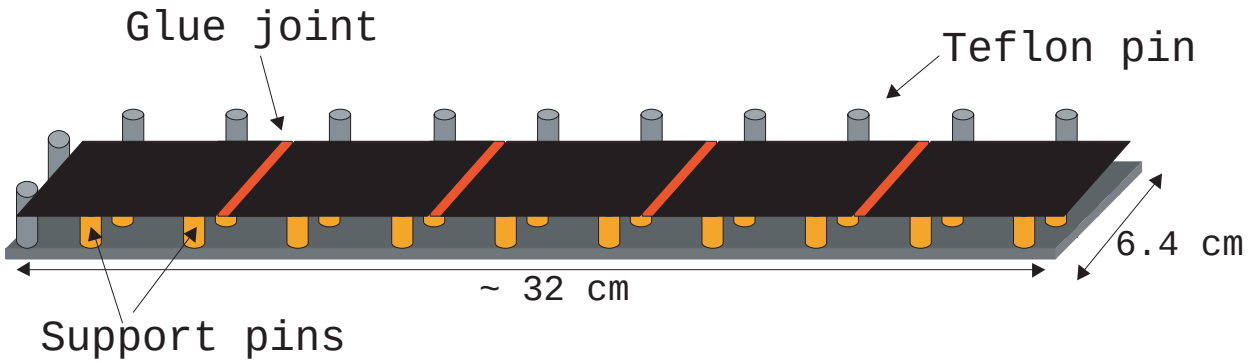

Figure 5: Schematic drawing of ladder assembly fixture

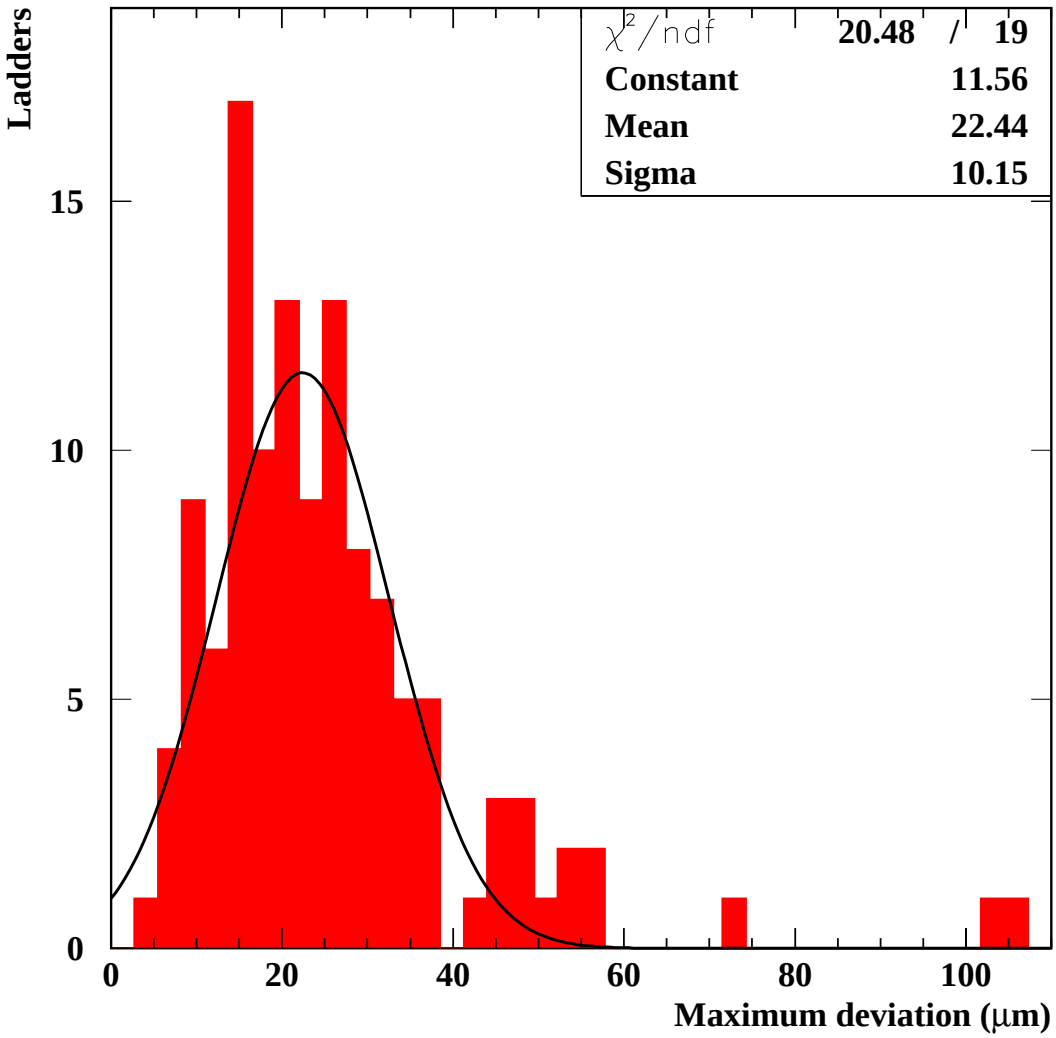

Figure 6: Alignment of detectors in a ladder (see text for explanation).

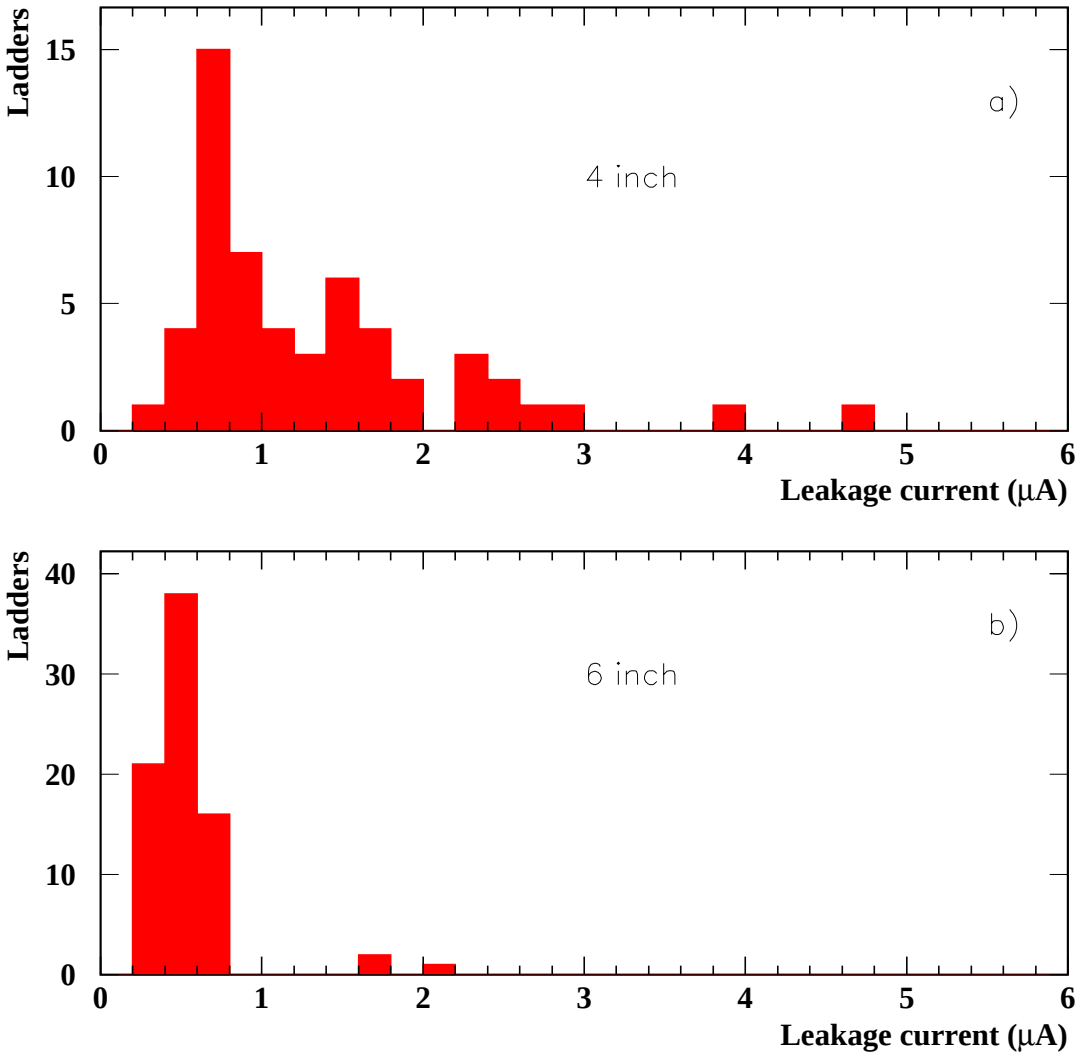

Figure 7: The measured leakage current for all Hamamatsu ladders after assembly.

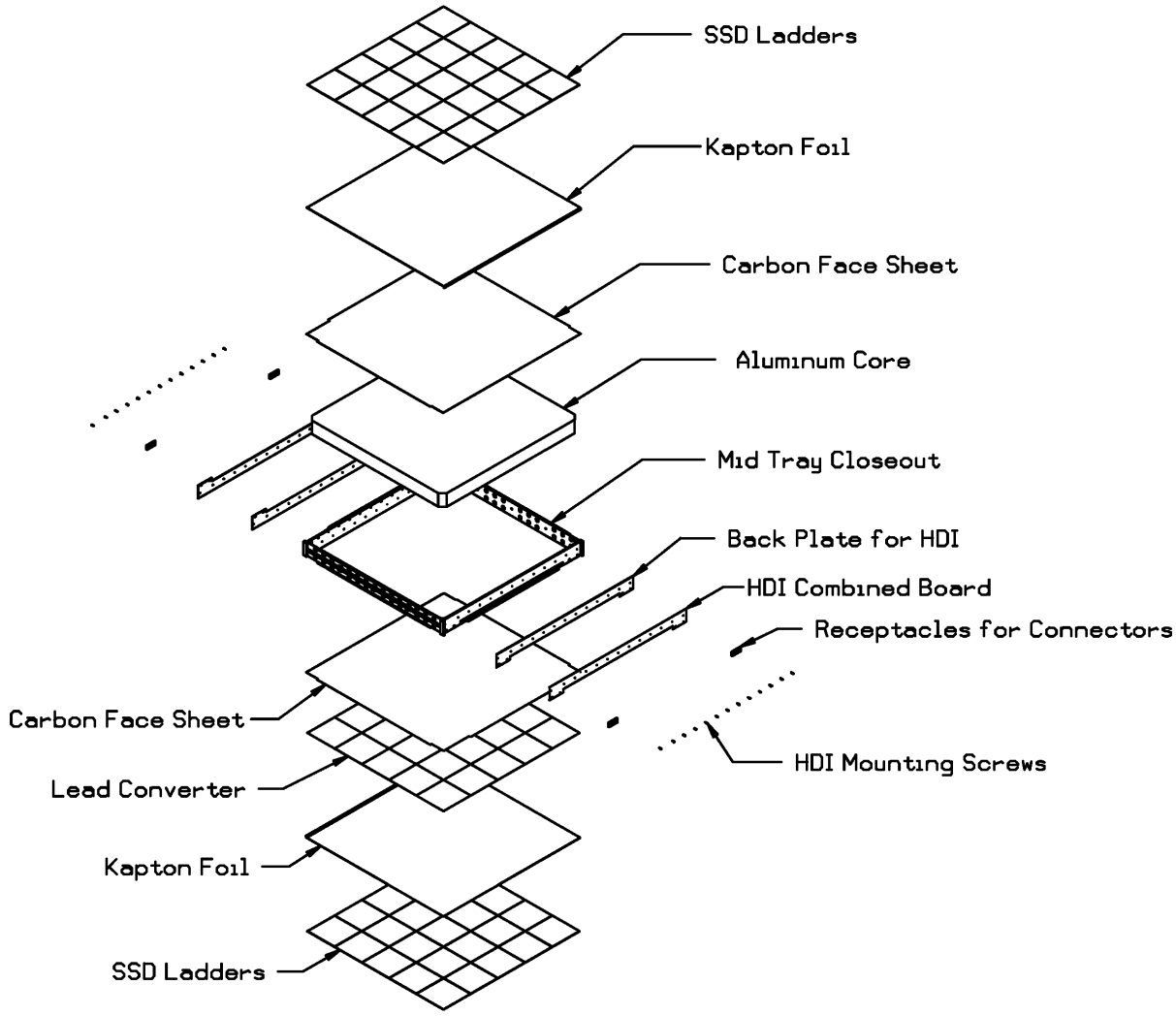

Figure 8: Exploded view of the mechanical layout of a tray.

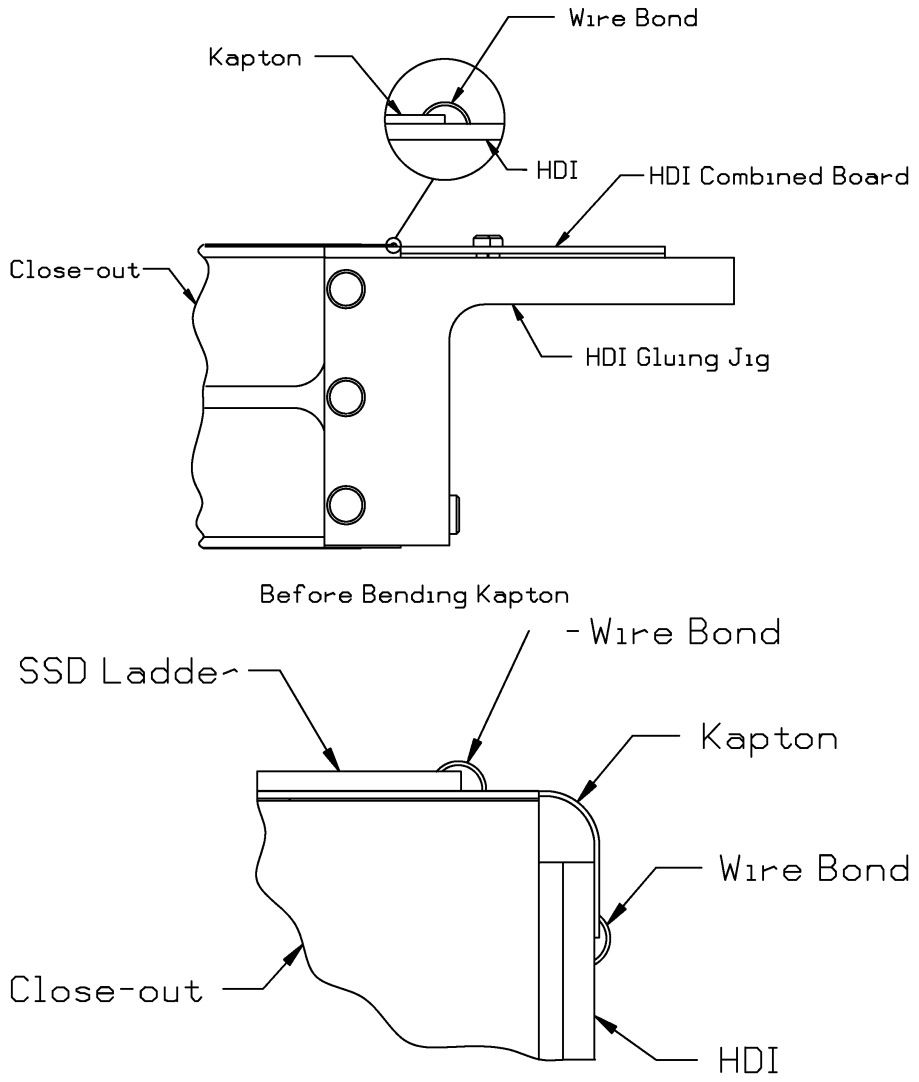

Figure 9: Schematic drawing describing the attachment of the electronic readout to the narrow edges of the trays before wire bonding (top), after wire bonding (bottom).

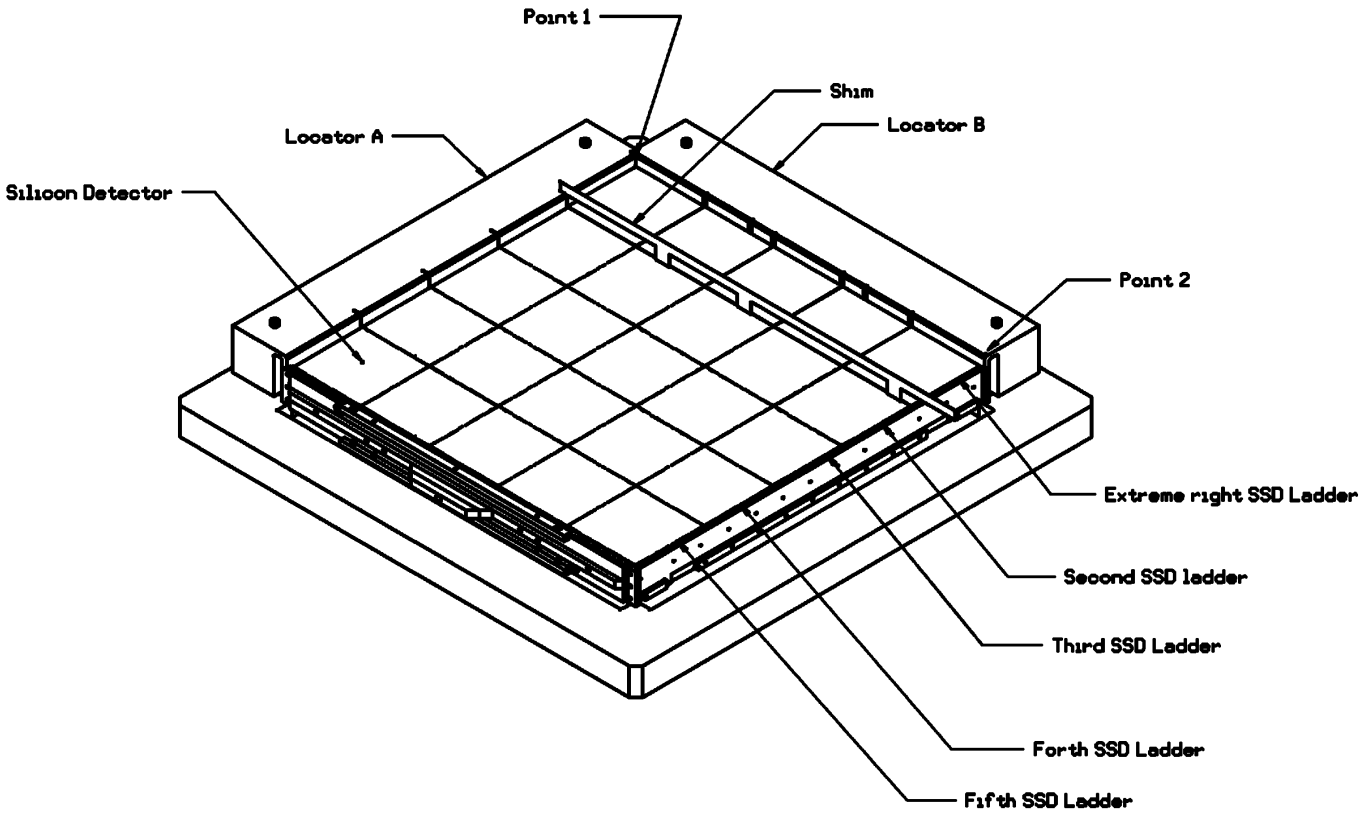

Figure 10: Schematic drawing of the fixture to mount ladders onto the trays before wire bonding to the kapton interconnect.

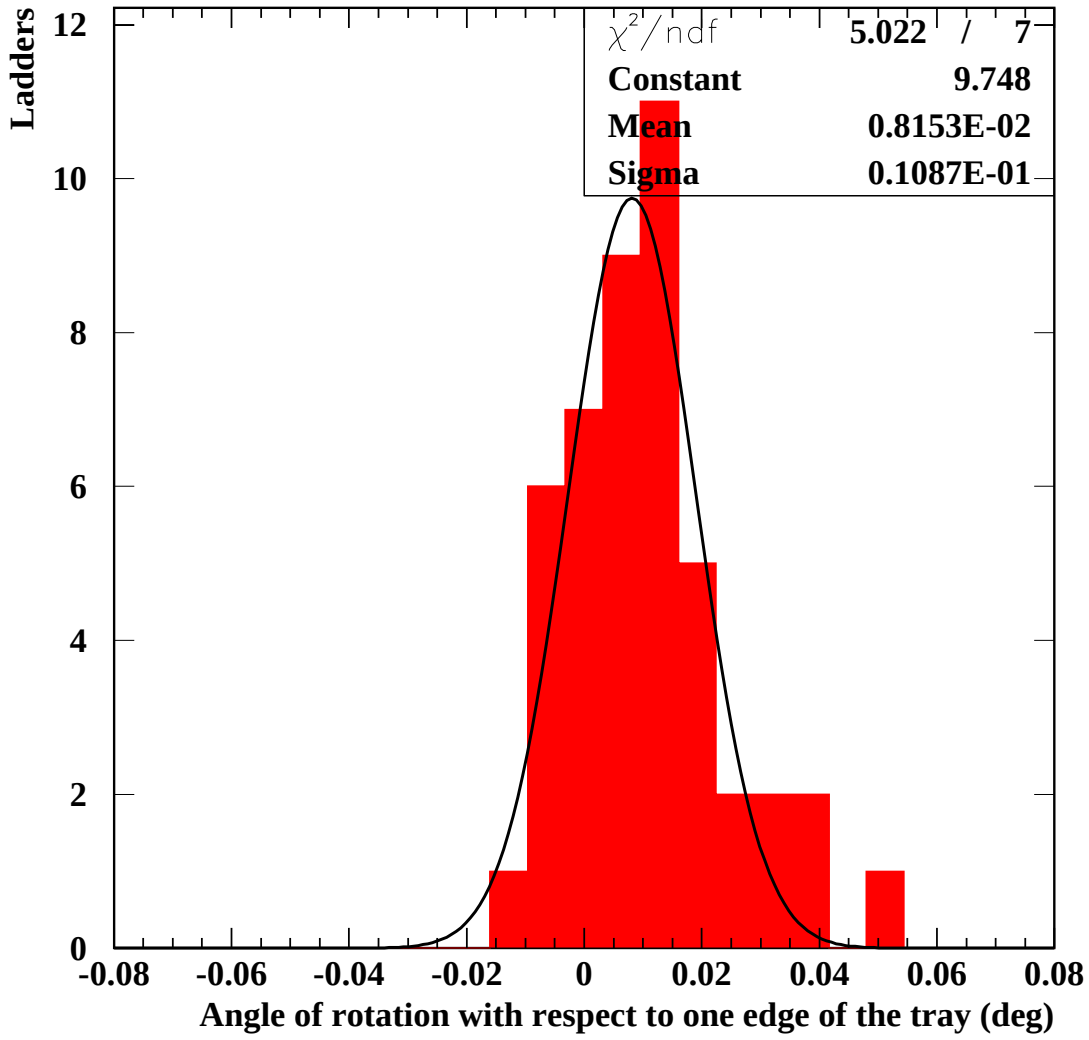

Figure 11: The angle of rotation in the xy plane for ladders mounted in trays (see definition in the text).

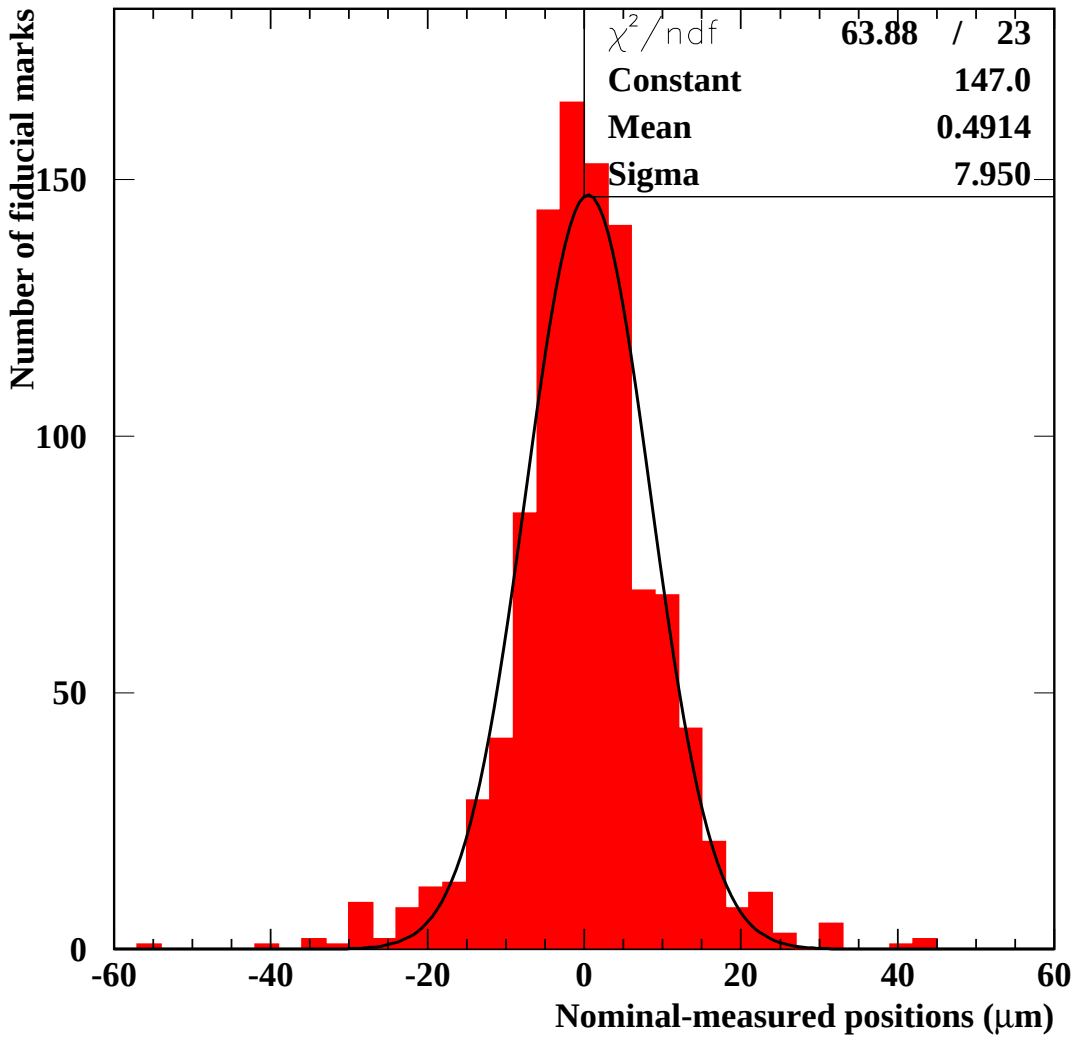

Figure 12: Nominal minus measured position in the direction perpendicular to the strips for all detector fiducial marks after assembly of ladders into trays.